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What is claimed is:

1. An insulating layer of a semiconductor device comprising:

about 5.25 - 5.75% by weight of boron; and

about 2.75 - 4.25% by weight of phosphorus.

2. The insulating layer as claimed in claim 1, wherein said insulating layer comprises a BPSG layer formed by adding said boron weight percentage and said phosphorus weight percentage into tetraethylorthosilicate (TEOS).

3. A method for forming an insulating layer comprising:

preparing an oxidizing atmosphere by supplying oxygen gas into a chamber to surround a substrate on which the insulating layer will be formed;

forming a first seed layer of said insulating layer on said substrate by supplying a tetraethylorthosilicate (TEOS) and the oxygen gas into the chamber;

forming a second seed layer of said insulating layer, said second seed layer capable of controlling an amount of boron added to said first seed layer by supplying triethylborate (TEB), the TEOS and the oxygen gas into the chamber; and

forming a BPSG layer as the insulating layer, which includes said first seed layer and said second seed layer, said BPSG layer capable of controlling the amount of the boron and phosphorus added thereto by supplying the TEB, the TEOS, triethylphosphate (TEPO), and an ozone gas into the chamber.

4. The method as claimed in claim 3, further comprising:

reflowing said insulating layer to evenly form an upper surface of said insulating layer using a hydrogen gas and the oxygen gas, and

simultaneously charging recessed regions with said insulating layer among elevated regions and recessed regions of a surface of said substrate.

5. The method as claimed in claim 3, wherein said first seed layer is formed by supplying the TEOS and the oxygen gas into the chamber with a mixed ratio of about 1: 5.4 to 5.8.

6. The method as claimed in claim 3, wherein said second seed layer is formed by supplying the TEOS, the TEB and the oxygen gas into the chamber with a mixed ratio of about 1:0.2 to 0.3:5.4 to 5.8.

7. The method as claimed in claim 3, wherein said BPSG layer is formed by supplying the TEOS, the TEB, the TEPO, and the ozone gas into the chamber with a mixed ratio of about 1:0.2 to 0.3:0.09 to 0.12:5.4 to 5.8.

8. The method as claimed in claim 3, wherein said oxidizing atmosphere, said first seed layer, said second seed layer and said BPSG layer are formed in a vacuum environment in the chamber, and wherein the vacuum environment is provided by supplying a helium gas and a nitrogen gas into the chamber with a mixed ratio of about

1:1.8 to 2.2.

9. The method as claimed in claim 3, wherein said insulating layer is formed after forming an etch stop layer on said substrate to prevent said substrate from being damaged by etching when said insulating layer is etched to form an insulating layer pattern having a window on said substrate.

10. A semiconductor device comprising:

a substrate having a gate electrode formed at an upper portion of said substrate, a source and a drain formed at a lower portion of both sides of said gate electrode; and

an insulating layer, to which about 5.25 - 5.75% by weight of boron and about 2.75-4.25% by weight of phosphorus is added, said insulating layer being continuously formed on said substrate and said gate electrode.

11. The semiconductor device as claimed in claim 10, further comprising an etch stop layer formed on said substrate.

12. The semiconductor device as claimed in claim 11, wherein said insulating layer includes a BPSG layer formed by adding the boron weight percentage and the phosphorus weight percentage to a tetraethylorthosilicate (TEOS).

13. A method for fabricating a semiconductor device comprising:

forming an etch stop layer on a substrate for preventing said substrate from being damaged by etching;

forming an insulating layer, to which about 5.25 - 5.75% by weight of boron and about 2.75 - 4.25% by weight of phosphorus is added, on said etch stop layer;

reflowing said insulating layer to evenly form an upper surface of said insulating layer, and simultaneously charging recessed regions with said insulating layer among elevated regions and recessed regions of said substrate; and

etching a predetermined portion of said insulating layer to form an insulating layer pattern having a window which exposes an upper surface of said underlying etch stop layer.

14. The method as claimed in claim 13, wherein said etch stop layer is comprised of nitride silicon and has a thickness within the range of from about 60 to about 140Å.

15. The method as claimed in claim 13, wherein said elevated regions and the recessed regions are formed by gate electrodes.

16. The method as claimed in claim 13, wherein said elevated regions and the recessed regions are formed by patterns having a window.

17. The method as claimed in claim 13, wherein said forming said insulating layer comprises:

preparing an oxidizing atmosphere by supplying oxygen gas into a chamber to surround a substrate on which the insulating layer will be formed;

forming a first seed layer on said substrate by supplying a tetraethylorthosilicate (TEOS) and the oxygen gas into the chamber with a mixed ratio of about 1:5.4 to 5.8;

forming a second seed layer on said first seed layer by supplying the TEOS, a triethylborate (TEB) and the oxygen gas into the chamber with a mixed ratio of about 1:0.2 to 0.3:5.4 to 5.8; and

forming a BPSG layer as the insulating layer, including said first seed layer and said second seed layer, by supplying the TEOS, the TEB, a triethylphosphate and an ozone gas into the chamber with a mixed ratio of about 1:0.2 to 0.3:0.09 to 0.12:5.4 to 5.8,

wherein said oxidizing atmosphere, said first seed layer, said second seed layer and said BPSG layer are formed in a vacuum environment, and

wherein the vacuum environment is provided by supplying helium gas and a nitrogen gas with a mixed ratio of 1:1.8 to 2.2.

18. The method as claimed in claim 13, wherein said insulating layer is formed to have a thickness within the range of about from 9,000 to 10,000Å.

19. The method as claimed in claim 13, wherein said insulating layer is etched by an etch gas having a CFx structure.

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